



Docket No.: 42390P10138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

MITSUHIRO ADACHI

Application No.: 09/749,088

Filed: December 26, 2000

For: **METHOD AND APPARATUS FOR
THERMAL THROTTLING OF CLOCKS**

Art Group: 2116

Examiner: James K. Trujillo

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INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted before the mailing of a final Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

07/15/2004 MBLANCO 00000018 09749088

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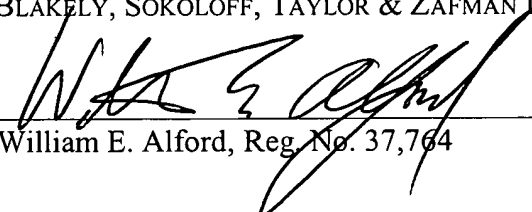
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

The fee set in the amount of \$180.00 for submission of the Information Disclosure Statement is enclosed herewith. Please charge any additional fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

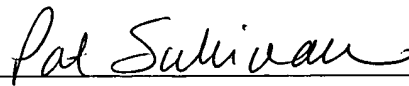
Date: July 12, 2004



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Pat Sullivan

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Date

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Complete if Known

Application Number	09/749,088
Filing Date	December 26, 2000
First Named Inventor	Mitsuhiro Adachi
Art Unit	2116
Examiner Name	James K. Trujillo
Attorney Docket Number	42390P10138

Sheet	1	of	2
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

[illegible]Examiner
Signature

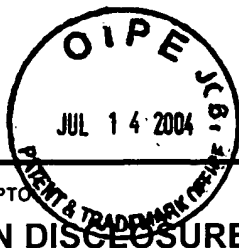
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Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08A (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 08/11/2003.

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	09/749,088
				Filing Date	December 26, 2000
				First Named Inventor	Mitsuhiro Adachi
				Art Unit	2116
				Examiner Name	James K. Trujillo
Sheet	2	of	2	Attorney Docket Number	42390P10138

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		JACOB MILLMAN, Ph.D., Charles Batchelor Professor, Emeritus, Columbia University, "Microelectronics, Digital and Analog Circuits and Systems," McGraw-Hill Book Co., 1979, pps. 673-676	
		RAYMOND M. WARNER, JR., Director of Engineering, Motorola Inc., Semiconductor Products Division, "Integrated Circuits, Design Principles and Fabrication," McGraw Hill Book Co., 1965, pps. 362-368	
		RAY P. PRASAD, SMT Program Manager, Intel Corporation, "Surface Mount Technology,, Principles and Practice," Van Nostrand Reinhold, New York, 1989, pps. 178-181	
		ADEL S. SEDRA, University of Toronto, KENNETH C. SMITH, University of Toronto and Hong Kong, "Microelectronic Circuits," 4th Ed., Oxford Univ. Press, 1998, pps. 773-778	
		"Intel486™ Microprocessor and Related Products," Microprocessors, PCIsets, Peripheral Components, Intel Corporation, 1995, pps. 2-304, 2-313 to 2-318	
		VLADIMIR ALEKSIEV, "Thermal Design for High Performance Notebooks," Intel Corporation, Order No. 241812-001, October 1993, pps. 2-493 to 2-508	
		CHENG XIE, MCG Technical Marketing, "Managing Power with the SL Enhanced Intel486™ Microprocessor," Intel Corporation, Order No. 241811-001, October 1993, pps. 2-485 to 2-490	
		PHILIP BRACE, "Clock Throttling the SL Enhanced Intel486™ CPU in a Networked Environment," Intel Corporation, Order No. 421988-001, May 1994, pps. 2-513 to 2-541	

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Examiner Signature		Date Considered	
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